UNITED STATES PATENT APPLICATION

GETTERING USING VOIDS
FORMED BY SURFACE TRANSFORMATION

INVENTORS
Leonard Forbes

Joseph Geusic

Schwegman, Lundberg, Woessner, & Kluth, P.A.
1600 TCF Tower
121 South Eighth Street
Minneapolis, Minnesota 55402
ATTORNEY DOCKET 1303.108US1
CLIENT REF. NO. 03-0414

GETTERING USING VOIDS FORMED
BY SURFACE TRANSFORMATION

Cross Reference To Related Applications

5   This application is related to the following commonly assigned U.S. patent applications which are herein incorporated by reference in their entirety: "Cellular Materials Formed Using Surface Transformation," Application Serial No. 10/382,246, filed March 5, 2003 (Attorney Docket 1303.086US1); "Gettering of Silicon On Insulator Using Relaxed Silicon Germanium Epitaxial Proximity

10   Layers," Application Serial No. 10/443,337, filed May 21, 2003 (Attorney Docket 1303.103US1); and "Wafer Gettering Using Relaxed Silicon Germanium Epitaxial Proximity Layers," Application Serial No. 10/443,339, filed May 21, 2003 (Attorney Docket 1303.104US1).

Technical Field

15

      This disclosure relates generally to integrated circuits, and more particularly, to strained semiconductor structures.

Background

20   Unwanted crystalline defects and impurities can be introduced during crystal growth or subsequent wafer fabrication processes. These defect and impurities can degrade device characteristics and overall yield. Gettering has been described as a process for moving contaminants and/or defects in a semiconductor into its bulk and away from its top surface to create a denuded zone cleared from contaminants

25   and/or defects. Preferably, devices are built in the denuded zone.

      Historically, extrinsic backside gettering was used to getter silicon wafers. Various extrinsic backside gettering processes involve damaging the backside of the wafer mechanically or by implanting argon, germanium, hydrogen or other implants, or providing a gettering layer on the backside of the wafer using a phophorosilicate

glass or oxide backside layer, a polysilicon backside layer, and a silicon germanium (SiGe) backside epitaxial layer. Subsequently, "intrinsic" gettering was developed, which employed oxygen precipitation and "bulk microdefects" precipitated into the bulk of the wafer after the surface was "denuded" of oxygen. The precipitation

5   process, the gettering effects, and the electrical characterization of defects and gettering silicon wafers have been investigated. Recently, intrinsic gettering modifications have been developed, including neutron irradiation, high boron doping, nitrogen doping, and the use of magnetic fields during crystal growth.

These gettering processes depend on the diffusion of unwanted impurities

10   over significant distances from desired device regions to the gettering sites. However, modern low temperature processes have small thermal budgets, and do not afford an opportunity for significant diffusion of dopants and/or unwanted impurities. Thus, it is desirable to reduce the distance between the gettering sites and the device area. It has been previously proposed to implant various impurities

15   in proximity to the device areas, to co-implant oxygen and silicon to form a gettering layer in close proximity to the device area, to implant helium to form cavities close to the device areas which getter impurities, and to getter material in trench isolation areas in close proximity to the device areas.

Implanting helium forms cavities that function to getter impurities. This

20   helium implantation technique has been proposed to getter both bulk and silicon-on-insulator devices. However, the location and density of these cavities formed by implanting helium is random. One problem associated with the random location and density of cavities is that the effectiveness of the gettering unwanted impurities from the desired device regions is inconsistent. Other problems associated with the

25   random location and density of cavities involves the varying strain in the substrate and the varying ability of the substrate to withstand mechanical strain. The inconsistent effectiveness of gettering, the inconsistent strain and the inconsistent ability to withstand strain can negatively affect the ability to precisely form devices

as the semiconductor industry strives to fabricate smaller and thinner devices.

Summary

The above mentioned problems are addressed and will be understood by reading and studying this specification. Various aspects and embodiments of the present invention getter a semiconductor wafer by precisely forming voids, such as nano-sized voids, at desired locations in the wafers. Thus, precisely-formed gettering void patterns are formed in selected regions below where devices are fabricated on semiconductor wafers. Numerous dangling bonds are present at the internal surfaces of the voids such that these internal surfaces are highly chemically reactive. Thus, various embodiments form the voids and void patterns to have a large surface to volume ratio to increase gettering of impurities.

One aspect of this disclosure relates to a method for creating a gettering site in a semiconductor wafer. In various embodiments, a predetermined arrangement of a plurality of holes is formed in the semiconductor wafer through a surface of the wafer. The wafer is annealed such that the wafer undergoes a surface transformation to transform the arrangement of the plurality of holes into a predetermined arrangement of at least one empty space of a predetermined size within the wafer to form the gettering site.

One aspect relates to a semiconductor wafer. In various embodiments, the wafer includes at least one device region, and at least one gettering region located proximate to the at least one device region. The gettering region includes a precisely-determined arrangement of a plurality of precisely-formed voids that are formed within the wafer using a surface transformation process. Other aspects and embodiments are provided herein.

This Summary is an overview of some of the teachings of the present application and not intended to be an exclusive or exhaustive treatment of the present subject matter. Further details are found in the detailed description and

appended claims. Other aspects will be apparent to persons skilled in the art upon reading and understanding the following detailed description and viewing the drawings that form a part thereof, each of which are not to be taken in a limiting sense. The scope of the present invention is defined by the appended claims and their legal equivalents.

Brief Description of the Drawings

Figure 1 illustrates a semiconductor structure having a gettering region with precisely formed voids at precise locations, according to various embodiments of the present invention.

Figure 2 illustrates a semiconductor structure having a gettering region with precisely formed voids at precise locations, according to various embodiments of the present invention.

Figure 3 illustrates a transistor formed in a device region proximate to a gettering region with precisely formed voids at precise locations, according to various embodiments of the present invention.

Figures 4A-4F illustrate a process to form a sphere-shaped empty space in a gettering region, according to various embodiments of the present invention.

Figures 5A-5C illustrate a process to form a pipe-shaped empty space in a gettering region, according to various embodiments of the present invention.

Figures 6A-6B illustrate a process to form a plate-shaped empty space in a gettering region, according to various embodiments of the present invention.

Figures 7A-7E illustrate the formation of empty spheres in a gettering region from initial cylindrical holes with the same radii and with varying length, according to various embodiments of the present invention.

Figure 8 illustrates a transformation formed stack of empty plates in a gettering region, according to various embodiments of the present invention.

Figure 9 illustrates fourteen representative unit cells of space lattices which the voids in the gettering region can form, according to various embodiments of the present invention.

Figure 10 illustrates a void pattern in a gettering region arranged to form the cubic P unit cell shown among the fourteen representative unit cells of Figure 9.

Figures 11A-11B illustrate a process for forming a cubic P lattice of spherical empty spaces, according to various embodiments of the present invention.

Figures 12A - 12D illustrate a process for forming a simple unit of empty spheres having two radii in a gettering region, according to various embodiments of the present invention.

Figure 13 illustrates a process for forming semiconductor devices, according to various embodiments of the present invention.

Figure 14 illustrates a process for precisely forming voids in a substrate located to getter a device region as performed in the process for forming semiconductor devices of Figure 13.

Figure 15 is a simplified block diagram of a high-level organization of a memory device, according to various embodiments of the present invention.

Figure 16 is a simplified block diagram of a high-level organization of an electronic system, according to various embodiments of the present invention.

Detailed Description

The following detailed description refers to the accompanying drawings which show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. The various embodiments are not necessarily mutually exclusive as aspects of one embodiment can be combined with aspects of another embodiment. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. In the following description, the terms wafer and substrate are

interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material,

5 combinations of such layers, as well as other such structures that are known in the art. The terms "horizontal" and "vertical", as well as prepositions such as "on", "over" and "under" are used in relation to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. References to "an", "one", or "various" embodiments in this disclosure are not

10 necessarily to the same embodiment, and such references contemplate more than one embodiment. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

15 Aspects of the present invention precisely form voids at desired location using a surface transformation process to getter semiconductor wafers. Various embodiments precisely form patterns of nano-voids (voids having a diameter on the order of a nanometer) as a proximity gettering region to effectively and consistently getter impurities from device regions.

20 Figure 1 illustrates a semiconductor structure having a gettering region with precisely formed voids at precise locations, according to various embodiments of the present invention. The illustrated structure 100 includes a semiconductor wafer, also referred to here as a substrate 101. A proximity gettering region 102 is located near to a device region 103 such that unwanted impurities can travel a short distance

25 from the device region 103 to the gettering region 102, even with modern low temperature processes. The gettering region 102 includes a number of precisely formed and located voids 104 formed by surface transformation. Surface transformation is described in detail below. The present invention is not limited to

gettering regions having a particular pattern, shape or size of voids. In various embodiments, the device region 103 includes crystalline silicon. Semiconductor devices, such as transistors, are fabricated in the crystalline silicon. Other crystalline semiconductor materials can be used to form the device region 103. Thus, it is

5   desired to getter unwanted impurities from the device region. The voids 104 in the gettering region 102 generate defects that getter impurities from the device region 103. The internal surfaces of the voids have numerous dangling bonds, and thus are highly chemically reactive, which serves to getter impurities from the device region 103.

10   Figure 2 illustrates a semiconductor structure having a gettering region with precisely formed voids at precise locations, according to various embodiments of the present invention. The illustrated structure 200 includes a semiconductor wafer, also referred to here as a substrate 201. A number of proximity gettering regions 202 are located near to a number of device regions 203 such that unwanted

15   impurities can travel a short distance from the device regions 203 to the gettering regions 202, even with modern low temperature processes. The gettering region 202 includes a number of precisely formed and located voids 204. The present invention is not limited to gettering regions having the illustrated pattern, size or shape of voids. The voids create defects that are highly chemically reactive and serve to

20   getter impurities from the device region 203.

Figure 3 illustrates a transistor formed in a device region proximate to a gettering region with precisely formed voids at precise locations, according to various embodiments of the present invention. The illustrated transistor 305 is fabricated over a proximity gettering region 302. The gettering region 302 has a

25   predetermined and precise arrangement of precisely formed voids 304. A gate oxide 306 is formed on the substrate 301, and a gate is formed over the gate oxide. First and second diffusion regions 308 and 309 are formed. A transistor channel region 310 is formed between the first and second diffusion regions 308 and 309. Other

devices, such as capacitors and diodes, can be formed in device regions proximate to a gettering region. These gettering regions and device regions can be formed in both bulk and semiconductor-on-insulator (SOI) technology. Furthermore, these gettering regions can be used to getter both strained and unstrained device regions.

5   In various embodiments, the precisely-determined arrangement of voids provides the gettering region with voids that are more uniformly spaced and with a majority of voids that are closed voids. The uniformity, density, and space symmetry of the voids in the gettering region is precisely determined by controlling the diameter, depth and position of an initial arrangement of cylindrical holes

10   formed through a surface of a solid (e.g. a surface of a semiconductor wafer). In various embodiments, the holes have a generally-elongated shape extending into the volume away from the surface. In various embodiments, the holes have a generally cylindrical shape. The present subject matter is not so limited, however.

        The voids in the gettering region generate defects that getter impurities from

15   the device region. The internal surfaces of the voids have numerous dangling bonds, and thus are highly chemically reactive which serves to getter impurities from the device region. Thus, various embodiments for voids and voids patterns to have a large surface to volume ratio to increase the gettering of impurities. In various embodiments, the precisely-determined arrangement of voids provides the

20   semiconductor wafer with a predictable mechanical failure for a given force. In various embodiments, the precisely-determined arrangement of voids provides the semiconductor wafer with an anisotropic stiffness.

        When a solid is heated to a higher temperature, a solid with a hole that is beyond a critical length (λ_c) becomes unstable. For the purposes of the analysis

25   provided below, the holes are referred to as cylindrical holes. Upon reading and comprehending this disclosure, one of ordinary skill in the art will understand that holes which are not geometrically cylindrical can be used in a surface transformation process, and further will understand how to form a predetermined arrangement of

voids using holes that are not geometrically cylindrical.

The cylindrical hole is transformed into one or more empty spheres formed along the cylinder axis. The number (N) of spheres formed depends on the length (L) and radius (R_C) of the cylinder. Two models of diffusion are the surface diffusion model and the pure volume diffusion model. With respect to the surface diffusion model, for example, the relation between the cylinder length (L), cylinder radius (R_C), and number of spheres (N) is expressed by the following equation:

$$(1) \qquad 8.89 \times R_c \times N \leq L < 8.89 \times R_c \times (N+1).$$

Equation (1) predicts that no empty spheres will form if L < 8.89 x R_C. Each empty sphere that forms has a radius (R_S) expressed by the following equation:

$$(2) \qquad R_S = 1.88 \times R_c.$$

If the cylinder has sufficient length L to form two spheres, the center-to-center spacing between the spheres corresponds to the critical length (λ_C) and is provided by the equation:

$$(3) \qquad \lambda_c = 8.89 \times R_c.$$

The pure volume diffusion model provides similar results, with slightly different constants. For example, depending on the exact magnitude of the diffusion parameters, λ_C can vary from 9.02 x R_C to 12.96 x R_C. One of ordinary skill in the art will understand, upon reading and understanding this disclosure, that the diffusion model is capable of being determined by experiment. The remainder of this disclosure uses the surface diffusion model. One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, how to apply this disclosure to another diffusion model.

Various shaped empty spaces or voids such as sphere-shaped voids, pipe-shaped voids, and plate-shaped voids are capable of being formed under the surface of a semiconductor substrate or wafer with a well-defined melting temperature. The shape of the empty spaces formed during the annealing conditions depends on the

size, number and spacing of the cylindrical holes that are initially formed at a lower temperature.

Various predetermined arrangements of empty spaces or voids are capable of being formed under the surface of a semiconductor substrate or wafer with a well-
5   defined melting temperature. For example, an appropriately-sized deep trench in a material with a well-defined melting temperature is transformed into empty spheres along the axis of the original trench at an annealing temperature within a predetermined a range below the melting temperature. The empty spheres are uniformly sized and spaced. Other predetermined arrangements are provided below.
10   Figures 4A-4F illustrate a process to form a sphere-shaped empty space in a gettering region, according to various embodiments of the present invention. A cylindrical hole 411 is formed through the surface 412 of a semiconductor volume where at least part of the volume forms a gettering region 402. As used here, the term hole refers to a void that extends from a surface of the volume into the solid
15   material and that is defined by the solid material. The semiconductor volume 402 is heated (annealed) and undergoes the transformation illustrated in Figures 4B through 4F. One of ordinary skill in the art would understand, upon reading and comprehending this disclosure, that the desired annealing temperature is dependent on the well-defined melting temperature of the semiconductor material. The result
20   of the surface transformation process is an empty sphere 413 formed below the surface 412 of the semiconductor volume 402.

In order to form a single sphere, which holds true for forming a single pipe (Figures 5A - 5C) or plate (Figures 6A - 6B), the length (L) and radius (R_C) of the cylindrical holes are chosen such that equation (1) with N = 1 is satisfied. A vertical
25   stacking of N empty spaces results if the length of the cylindrical holes is such that equation (1) is satisfied.

In order for single surface-transformed spheres to combine with other surface-transformed spheres, the center-to-center spacing (D_{NT}) between the initial

cylindrical holes will satisfy the following equation:

$$(4) \qquad 2 \times R_C < D_{NT} < 3.76 \times R_C.$$

Satisfying this equation prevents the adjacent initial cylindrical holes from touching, yet allows the adjacent surface-transformed spheres to combine and form pipe and plate empty spaces, as shown in Figures 5A-5C and Figures 6A-6B and described below.

Figures 5A-5C illustrate a process to form a pipe-shaped empty space in a gettering region, according to various embodiments of the present invention. A linear array of cylindrical holes 511 is formed through a surface 512 of a semiconductor volume where at least part of the volume forms a gettering region 502. The cylindrical holes 511 have a center-to-center spacing (D_{NT}) as calculated using equation (4). The semiconductor material 502 is heated (annealed) and undergoes the transformation illustrated in Figures 5B through 5C. The result of the surface transformation process is an empty pipe-shaped void 514 formed below the surface 512 of the semiconductor volume 502. The radius (R_P) of the pipe-shaped void 514 is provided by the following equation:

$$(5) \qquad R_P = \sqrt{\frac{8.86 \times R_C{}^3}{D_{NT}}}.$$

Figures 6A-6B illustrate a process to form a plate-shaped empty space in a gettering region, according to various embodiments of the present invention. A two-dimensional array of cylindrical holes 611 is formed in a surface 612 of a semiconductor volume where at least part of the volume forms a gettering region 602. The cylindrical holes 611 have a center-to-center spacing (D_{NT}) as calculated using equation (4). The material 602 is heated (annealed) and undergoes the transformation illustrated in Figures 6B. The result of the surface transformation process is an empty plate-shaped void 615 formed below the surface 612 of the volume of material 602. The thickness (T_P) of a plate 320 is given by the following

equation:

$$(6) \quad T_P = \frac{27.83 \times R_C{}^3}{D_{NT}{}^2}$$

The voids are formed in a gettering region using surface transformation. In various embodiments, a precisely-determined arrangement of voids is formed using surface transformation to provide a large interior void surface to volume ratio and to provide a desired distribution of the voids throughout the gettering region. In various embodiments, the voids in the gettering region include nano-sized voids ("nano-voids"). In various embodiments, the present subject matter forms a precisely-determined arrangement of voids using surface transformation to provide a cellular material with a predictable mechanical failure for a given force. In various embodiments, the present subject matter forms a precisely-determined arrangement of voids using surface transformation to provide a cellular material with an anisotropic stiffness.

The size, shape and spacing of empty spaces is controlled by the diameter, depth and spacing of holes (or trenches) initially formed in a semiconductor material that has a defined melting temperature. Empty spaces or voids are formed after annealing the material in a temperature range below and near the defined melting temperature. The empty spaces or voids are capable of being formed with a spherical shape, a pipe shape, plate shape, various combinations of these shape types, and/or various dimensions for the various shape type and combinations of shape type. The volume of air incorporated in the surface transformed empty spaces is equal to the volume of air within the initial starting pattern of cylindrical holes. Thus, the surface transformed empty spaces do not cause additional stress in the material or a tendency for the material to crack.

The surface of the semiconductor volume will be smooth after the surface transformed empty spaces are formed if the initial cylinder length (L) is equal to an integer of a critical length (λ_c) such as 1 x λ_c to form one sphere, 2 x λ_c to form two

spheres, 3 x λ_c to form three spheres, etc.. If the cylinder length (L) is not equal to an integer of a critical length (λ_c), then the surface will have dimples caused by air in the cylinder attributable to the length beyond an integer of a critical length (λ_c). That is, for a given length L and λ_c, the number of spheres formed is the integer of L/λ_c, and the remainder of L/λ_c contributes to the dimples on the surface.

Figures 7A-7E illustrate the formation of empty spheres in a gettering region from initial cylindrical holes with the same radii and with varying length, according to various embodiments of the present invention. Initial cylindrical holes are represented using dashed lines 711. These initial cylindrical holes 711 have the same radius (R_C) and are drilled or otherwise formed to different depths as represented by Figures 7A, 7B, 7C, 7D and 7E. The resulting surface-transformed spheres 713 are illustrated with a solid line, as are the surface dimples 716 that form when the cylindrical hole depth is not an integer multiple of λ_C. These surface dimples can be removed using a simple polishing process to leave a smooth surface with uniform and closed spherical voids within the material. A crystalline semiconductor can be formed over the polished gettering region for use in fabricating semiconductor devices. The vertical position and number of the spherical voids is determined by the depth of the initial cylindrical holes.

In various embodiments of the present subject matter, the gettering region of the semiconductor substrate is formed by appropriately spacing the initially-formed holes such that, upon annealing the semiconductor material to provide the surface transformation process, the resulting voids are uniformly spaced (or approximately uniformly spaced) throughout the gettering region. The uniformly spaced voids provide the gettering region with the ability to getter a device region with more uniformity. Smaller voids provide more gettering uniformity. With more predictable gettering of device regions, the performance of the devices formed therein is more predictable, thus providing better yield.

In various embodiments, it is desirable to provide a gettering region with

voids to provide a high internal void surface to volume ratio to improve gettering. The interior void surfaces have dangling bonds that are highly chemically reactive, and are useful to getter impurities.

Figure 8 illustrates a transformation formed stack of empty plates 815 in a gettering region 802, according to various embodiments of the present invention. For example, the illustrated filling factor, f, is approximately equal to 0.78, which provides a relatively high porosity, a relatively low density, and a relatively high internal void surface to volume ratio. In the illustrated example, the surface transformation produces a vertical stack of empty plates in the materials. The number of empty plates formed depends on the length of the holes. Various embodiments of the vertical stack includes one ore more empty plates. From equation (6), it is determined that the thickness T_P of the empty plate has a maximum value of 6.95 x R_C when D_{NT} is near the minimum allowed value of 2 x R_C as inferred from equation (4). From equation (3), the center-to-center spacing (λ) of empty plates is 8.89 x R_C. It can be calculated that f $\approx$0.78.

In various embodiments of the present subject matter, a plurality of space group symmetries of empty spheres of equal size are formed in a solid material.

Figure 9 illustrates fourteen representative unit cells of space lattices which the voids in the gettering region can form, according to various embodiments of the present invention. For simplicity, only the cubic P unit cell of Figure 9 with a lattice constant "a_0" is discussed below. One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, how to form void patterns for the other unit cells illustrated in Figure 9. Each void in the unit cell can be the same shape (e.g. sphere-shaped, plate-shaped or pipe-shaped voids). In various embodiments, the unit cell includes different combinations of sphere-shaped, plate-shaped, or pipe-shaped voids.

Figure 10 illustrates a void pattern in a gettering region arranged to form the cubic P unit cell shown among the fourteen representative unit cells of Figure 9. A

defined set of cylindrical holes are drilled or otherwise formed into the gettering region to form empty spheres 1013 of the same radius in the solid material at each of the illustrated unit cell lattice positions. For simplicity, the formation of one unit cell in the x - y plane and n unit cells in the z direction is discussed. Additional unit

5 cells in the x - y planes are formed by repeatedly translating the hole pattern for the unit cell in the x and y directions. From equations (2) and (3), spheres are created with periodicity a_0 in the Z direction by drilling or otherwise forming the holes in the Z direction such that the radius of the holes (R_C) are represented by the following equation:

10 (7) $\quad R_C = \dfrac{a_0}{8.89} \approx 0.11 \times a_0.$

After surface transformation, the radius, R_S of each formed empty sphere is:

(8) $\quad R_S = \dfrac{1.88}{8.89} \times a_0 \approx 0.212 \times a_0.$

In order to form n unit cells in the Z direction through surface transformation, the depth (L_n)of the initial cylinder in the Z direction is:

15 (9) $\quad L_n = (n+1) \times a_0 = (n+1) \times 8.99 \times R_C.$

To form a single cubic P unit cell in the Z direction, n is set to 1 for the two deep arrangement of spheres such that the cylindrical holes are formed to the following hole depth:

(10) $\quad L_1 = 2 \times 8.89 \times R_C = 2 \times a_0.$

20 Figures 11A-11B illustrate a process for forming a cubic P lattice of spherical empty spaces, according to various embodiments of the present invention. Referring to Figure 11A, four cylindrical holes 1111A, 1111B, 1111C and 1111D of radius Rc = 0.11 x a_0 are formed into the semiconductor volume 1102 from a surface 1112 to a depth L = 2 x a_0. The four cylindrical holes 1111A, 1111B, 1111C

25 and 1111D are spaced apart along the x and y axes at a distance a_0. The solid

material is annealed near its melting temperature to form sphere-shaped empty spaces 1113A, 1113B, 1113C, 1113D, 1113E, 1113F, 1113G and 1113H by surface transformation at desired sites of the cubic P unit cell as is shown in Figure 11B.

One of ordinary skill in the art will understand, upon reading and
5   comprehending this disclosure, that the unit cells of each primitive lattice in Figure 6 can be formed to have equal sized empty spheres at each lattice site by forming in the Z direction an appropriate pattern of cylindrical holes of the same diameter in the x-y plane. The prescribed depths for these unit cells will generally be different.

In various embodiments, space lattices having more than one size of empty
10   spheres in the unit cell are formed by forming initial cylindrical holes of more than one radius. In various embodiments, the holes are formed in more than one direction. The number of surface transformation annealing steps used to form the space lattice depends on the structure to be formed. A method to form a simple illustrative structural unit of empty spheres is described below.

15   Figures 12A - 12D illustrate a process for forming a simple unit of empty spheres having two radii in a gettering region, according to various embodiments of the present invention. The desired structure has four empty spheres of radius $R_S = 0.212 \times a_0$, and four empty spheres of radius $R_{S'} = \frac{1}{2} \times R_S = 0.106 \times a_0$. All of the empty spheres have a closest center-to-center spacing of $a_0/2$. The process to form
20   the above-described structure is illustrated in Figures 12A, 12B, 12C and 12D.

In Figure 12A, two cylindrical holes 1211A of radius, $R_C = 0.11 \times a_0$ and of length $L = 2 \times a_0$ are formed in the Z direction. The solid material is annealed to effect surface transformation and form the four spheres 1213A with $R_S = 0.212 \times a_0$, as shown in Figure 12B.

25   In Figure 12C, two cylindrical holes 1211B are drilled in the y-direction. These holes 1211B have a radius $R_{C'} = 0.055a_0$, and a length $L' = a_0$. Again the material is annealed to effect surface transformation and the four smaller empty spheres 1213B to form the desired structure shown in Figure 12D. The second

annealing step only effects the cylindrical holes since they are not energetically stable. The four previously formed larger empty spheres are stable since they were formed during the first annealing.

Another method for forming the structure in Figure 12D involves forming the cellular material in various deposition layers and forming the voids using a surface transformation process (*i.e.* hole formation and annealing) for each layer before a successive layer of material is deposited. Using this method, the structure illustrated in Figure 12D is formed by a first deposition process, a first surface transformation process, a second deposition process, a second surface transformation process, a third deposition process, a third surface transformation process, a fourth deposition process, and a fourth surface transformation process. Each surface transformation step includes hole formation and annealing. For each layer, the hole formation pattern is calculated to achieve the desired spacing of resulting voids, both between and within layers, after the layer is annealed.

One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that a number of void arrangements are capable of being formed, a number of void sizes are capable of being formed, and that various combinations of void arrangements and void sizes are capable of being formed. One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that various different shapes of empty spaces can be formed, and that these various different shapes of empty spaces can be combined with other shapes of empty spaces. For example, a cellular material can include a number of sphere-shaped voids, a number of pipe-shaped voids, a number of plate-shaped voids, and various combinations of sphere-shaped void(s), pipe-shaped void(s), and plate-shaped void(s). One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that the various shapes can be stacked, and that various different shapes can be stacked together. For example, an arrangement of spheres can be stacked on top of an arrangement of plates. Additionally, each stack

of voids can include various shapes. The precisely-determined arrangement of empty spaces is determined by the position, depth and diameter of the holes formed prior to the annealing process.

The figures presented and described above are useful to illustrate method aspects of the present subject matter. Some of these method aspects are described below. The methods described below are nonexclusive as other methods may be understood from the specification and the figures described above.

Figure 13 illustrates a process for forming semiconductor devices, according to various embodiments of the present invention. At 1320, voids are precisely formed and are located to getter a device region. At 1321, subsequent semiconductor fabrication processes are performed, As represented at 1322, these subsequent semiconductor fabrication processes include forming a semiconductor device in a device region. An example of a semiconductor device is a transistor. In various embodiments, these semiconductor processes include depositing a semiconductor such as crystalline silicon on the gettering region, and forming a transistor using the crystalline silicon. In various embodiments, the voids are formed in a crystalline semiconductor volume, and the devices are formed using the crystalline semiconductor above the voids. In various embodiments, the voids are formed in a crystalline semiconductor volume, and the devices are formed using the crystalline semiconductor adjacent to the voids.

Figure 14 illustrates a process for precisely forming voids in a substrate located to getter a device region as performed in the process for forming semiconductor devices of Figure 13. The illustrated process 1420 generally corresponds to the 1320 in Figure 13. In the illustrated embodiment, holes are formed to extend from a substrate surface and into a semiconductor substrate at 1423. The holes have a predetermined size and shape, and are formed in a predetermined location or pattern of locations in the substrate. In various embodiments, the holes have a generally cylindrical shape. At 1424, the substrate is

annealed to form predetermined voids in the substrate. The substrate has a well-defined melting temperature, and the annealing temperature is slightly below the melting temperature. Depending on the size, shape and pattern of holes formed at 1423, the voids can include sphere-shape voids, a pipe-shape voids and/or plate-shaped voids.

The present subject matter provides the ability to form gettering regions with a precisely-determined arrangement of precisely-formed voids using surface transformation. In various embodiments, the precisely-determined arrangement of precisely-formed voids include uniformly spaced and closed voids that provide the gettering region with uniform gettering characteristics and with a large internal surface to volume ratio to provide a large number of uniformly distributed dangling bonds (defects in the crystalline structure) in proximity to a device region to effectively getter the device region. Thus, by effectively removing impurities from device regions, semiconductor devices are cable of being precisely fabricated.

SYSTEM LEVEL

Figure 15 is a simplified block diagram of a high-level organization of a memory device, according to various embodiments of the present invention. The illustrated memory device 1530 includes a memory array 1531 and read/write control circuitry 1532 to perform operations on the memory array via communication line(s) 1533. The illustrated memory device 1530 may be a memory card or a memory module such as a single inline memory module (SIMM) and dual inline memory module (DIMM). One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that semiconductor components in the memory array 1531 and / or the control circuitry 1532 are able to be fabricated using the gettering regions having precise patterns of voids formed by surface transformation, as described above.

The memory array 1531 includes a number of memory cells 1534. The memory cells in the array are arranged in rows and columns. In various embodiments, word lines 1535 connect the memory cells in the rows, and bit lines 1536 connect the memory cells in the columns. The read/write control circuitry 1532 includes word line select circuitry 1537, which functions to select a desired row. The read/write control circuitry 1532 further includes bit line select circuitry 1538, which functions to select a desired column.

Figure 16 is a simplified block diagram of a high-level organization of an electronic system, according to various embodiments of the present invention. In various embodiments, the system 1640 is a computer system, a process control system or other system that employs a processor and associated memory. The electronic system 1640 has functional elements, including a processor or arithmetic/logic unit (ALU) 1641, a control unit 1642, a memory device unit 1643 (such as illustrated at 1530 in Figure 15) and an input/output (I/O) device 1644. Generally such an electronic system 1640 will have a native set of instructions that specify operations to be performed on data by the processor 1641 and other interactions between the processor 1641, the memory device unit 1643 and the I/O devices 1644. The control unit 1642 coordinates all operations of the processor 1641, the memory device 1643 and the I/O devices 1644 by continuously cycling through a set of operations that cause instructions to be fetched from the memory device 1643 and executed. According to various embodiments, the memory device 1643 includes, but is not limited to, random access memory (RAM) devices, read-only memory (ROM) devices, and peripheral devices such as a floppy disk drive and a compact disk CD-ROM drive. As one of ordinary skill in the art will understand, upon reading and comprehending this disclosure, any of the illustrated electrical components are capable of being fabricated to include the silicon germanium proximity gettering region in accordance with various embodiments of the present invention.

The illustration of the system 1640 is intended to provide a general understanding of one application for the structure and circuitry, and is not intended to serve as a complete description of all the elements and features of an electronic system using proximity gettering regions according to the various embodiments of

5   the present invention. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

Applications containing a gettering region as described in this disclosure

10   include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems.

15   **CONCLUSION**

Various embodiments disclosed herein getter a semiconductor wafer by precisely forming voids, such as nano-voids, at desired locations in the wafers. Various embodiments form an even distribution of voids across the wafer below device regions. In various embodiments, precisely-formed gettering void patterns

20   are formed proximate to selected regions where devices are fabricated on the semiconductor wafer. Various embodiments precisely form the void patterns below device regions. Numerous dangling bonds are present at the internal surfaces of the voids such that these internal surfaces are highly chemically reactive. Thus, various embodiments form the voids and void patterns to have the greatest surface to

25   volume ratio to increase the gettering of impurities.

This disclosure includes several processes, circuit diagrams, and structures. The present invention is not limited to a particular process order or logical arrangement. Although specific embodiments have been illustrated and described

herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover adaptations or variations. It is to be understood that the above description is intended to be

5   illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments, will be apparent to those of skill in the art upon reviewing the above description. The scope of the present invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.